REMARKS

Claims 1-16 are presented for further examination. Claims 1-7 have been amended, and claims 8-16 are new.

In the Office Action mailed September 24, 2003, the Examiner requested amendment to the figures wherein Figure 1 should be designated by a legend such as "Prior Art." Applicants are submitting herewith proposed drawing corrections to Figure 1 wherein the legend "Prior Art" has been added. Approval and entry of this drawing is respectfully requested.

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,339,011 ("Tamura et al.") in view of prior art Figure 1 in the instant application. Remarks accompanying the rejection state that while Tamura et al. does not explicitly say that the comparator has a plurality of comparator circuits, the claimed limitation is found in Figure 1 of the instant application, which the Examiner asserts as showing a comparator having a plurality of comparator circuits as claimed. Applicants respectfully disagree with the basis for the rejection and request reconsideration and further examination of the claims.

In both Figure 1 and Figure 4 of the application, the cut-off control loop circuit shows an up/down counter coupled to the output of a comparator. In the case of Figure 4, a speeding circuit is inserted between the counter and the comparator. Both figures also show two additional comparators, one configured to generate the reference current and the other configured to generate a warm-up voltage. The latter two comparators do not have outputs coupled to the speeding circuit, as shown in Figure 4 and as recited in the claims. Moreover, as recited in claim 1 and shown in Figure 4, the speeding circuit has an input coupled to only the output of the speeding comparator circuit. The outputs of the other two comparators coupled in parallel with the speeding comparator circuit are not coupled to the input of the speeding circuit.

Tamura et al. is directed to a display device that utilizes a single comparator (17) that cannot give a measure of the difference between regulated level and target and level, and does not enable a blanking control in the manner provided by the present invention. Moreover, in Tamura et al. the blanking depends on a detection of current in the three guns (see Tamura et al. column 12, lines 43-66, and Figure 11, and operation with cathode current) and a timer as described at column 13, lines 2-4: "the CRT is judged to be in stable condition." This detection

of current in Tamura et al. would correspond to a voltage on the comparator input Vcut-off higher than Vleak for Icbpositive. (See instant application equation P4.) The speeding comparator of the present invention enables more accurate determination of when to unblank with a level that is closer to the regulation level. A timer is not needed and thus unblanking is faster, which is a purpose of the invention.

Turning to the claims, claim 1 is directed to an RGB control circuit for use in television/video display control having a display driver current sensor; a counter circuit and analog output circuit coupled to control the display driver current; a speeding comparator having a plurality of comparator circuits coupled in parallel with the display driver current sensor as input for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof. Nowhere does Tamura et al. teach or suggest a plurality of comparator circuits coupled in parallel with a display driver current sensor to function as a speeding comparator as recited in claim 1. Moreover, claim 1 further recites a speeding logic circuit having an input coupled to an output of the speeding comparator and further having an output coupled to an input of the counter circuit and arranged to control up/down counting of the counter circuit according to a measure of the difference in display driver current. Again, there is no teaching or suggestion in Tamura et al. of a speeding logic circuit having an input coupled to an output of the speeding comparator and an output coupled to an input of the counter circuit. Moreover, in Tamura et al. the comparator (17) does not have an output coupled to an intermediate speeding circuit that in turn has an output coupled to a counter circuit as recited in the combination of claim 1. For these reasons, applicants respectfully submit that claim 1, and all claims depending therefrom, are clearly allowable.

New claims 8 and 9 recite the additional comparators with their respective functions, which are clearly distinct from the speeding comparators recited in claim 1. Nowhere does Tamura et al. or Figure 1 of the present application, taken alone or in any combination thereof, teach or suggest the features of these claims.

Independent claim 10 is directed to a control circuit that includes the counter circuit having an output coupled to a digital-to-analog converter and a speeding circuit coupled to an input of the counter circuit and receiving an output signal from a speeding comparator

having a plurality of comparator circuits. Nowhere does Tamura et al. teach or suggest such a configuration as discussed above with respect to Figure 1. Applicants respectfully submit that claim 10 and corresponding dependent claims are clearly allowable for the reasons why claim 1 is allowable.

Claim 14 includes limitations similar to claim 1 with respect to the comparator circuit comprising a plurality of comparator circuits that are separate and distinct from the comparators used for the reference current generator and the warm-up mode comparator that receives the referenced starting voltage. Applicants respectfully submit that claim 14 and all claims depending therefrom are allowable over the combination of Tamura et al. and Figure 1 of the present application.

In view of the foregoing, applicants submit that all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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ERT:jl
Enclosure:
Postcard
1 Sheet of Drawings (Figure 1)

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